Fairchild Imaging CCD 10121

12K x 128 Element, Time Delay Integration Sensor

GENERAL DESCRIPTION

The CCD 10121 is a 12,288 pixel x 128 line, high speed TDI sensor. The active imaging area is organized as 12,288 vertical columns and 128 horizontal TDI rows. The array is set up for bi-directional operation. There are identical output registers and amplifiers on both the top and the bottom of the array. The outputs to be used (either top or bottom) are user-selectable and controlled by the vertical clock timing. In addition, the exposure level can be controlled by reducing the number of TDI rows from 128 to 96, 64, 32, 16, 8 or 4. This is also user-selectable and is accomplished by supplying the appropriate phasing for the vertical clocks within each section. For instance, if 64 lines of TDI were required, the vertical clocks for lines 65-128 would be connected to a high potential, which would drain these unused rows out to the opposite side (unused) of the array to be dumped into the VOFD drain. With eight outputs, each running at 20MHz, the CCD 10121 can provide a total data rate of 160MHz enabling the CCD to run at better than 12kHz line rate. Utilizing Fairchild Imaging proprietary buried channel CCD process, the CCD 10121 achieves consistent, superior TDI performance.

The active imaging area is separated from the eight horizontal output registers by 21 isolation rows. These isolation rows are covered by a metal lightshield to protect them while charge transfers to the output registers. Both the active imaging area and the isolation region utilize 3-phase clocking.

The eight horizontal output registers utilize 4-phase clocking. Special design techniques have been implemented to maximize charge transfer efficiency especially at low light levels. The output amplifier is a 3-stage source follower configuration. This allows maximum scale factor (charge to voltage conversion) and maximum bandwidth.

The CCD 10121 is housed in a custom 480 pin (100 mil grid) ceramic PGA package. It has an AR coated window.

FEATURES

- 12,288 pixels per line
- **Number of TDI stages electronically selectable: { 4, 8, 16, 32, 64, 96, 128 }**
- **Bi-directional TDI (shift up or down)**
- 8 outputs – each capable of 20MHz data rate – 160MHz total data rate
- 100% fill factor
- 8.75µm x 8.75µm pixel size
- On-chip binning capability

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: These are elements of a line of 12,288 image sensors separated by channel stops and covered by a passivation layer. Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

Transfer Gates: This gate is a structure adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gate to the transport shift registers whenever the transfer gate voltage goes high.

Shift Registers: The vertical shift register is 3-phase and the horizontal shift register is 4-phase.

Time Delay and Integration: This function is accomplished by scanning the image scene across the array at the same rate as the vertical shift register moves the signal charge. This results in an effective increase in the integration time.

Output Amplifier: The CCD 10121 is designed for either uni-directional or bi-directional operation. There are eight identical output registers and amplifiers on both the top and bottom of the array. There are three-stage source follower amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ϕR to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

DEFINITION OF TERMS

Charge-Coupled Device: A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Isolation Rows: There are 21 isolation rows between the image area and the horizontal shift register. These non-imaging rows are used as buffer rows to eliminate crosstalk to the horizontal shift register.

Dynamic Range: The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

RMS Noise Equivalent Exposure: The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposure: The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Charge Transfer Efficiency: Percentage of valid charge information that is transferred between each successive stage of the transport register.

Responsivity: The output signal voltage per unit of exposure.

Photo-Response Non-Uniformity: The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal: The output signal caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Integration Time: The time interval between the falling edges of any two successive transfer pulses is the integration time shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel: Picture element or sensor element, also called photoelement or photosite.

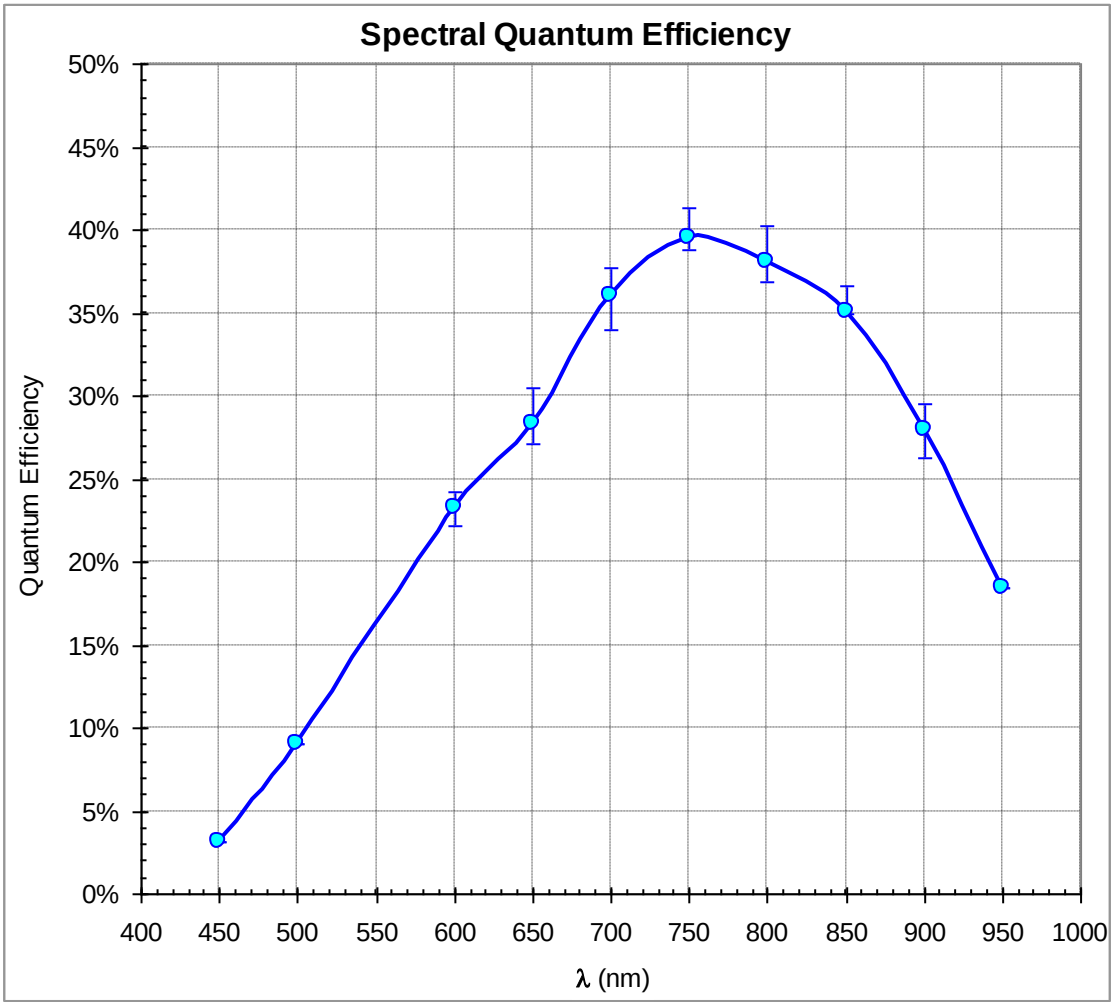
CCD 10121 Device Architecture	
Pixel array (across-the-TDI-scan)	12,288 pixels per line = 8 sectors x 1,536 pixels/sector
Pixel array (along-the-TDI-scan)	Clock-selectable: {4, 8, 16, 32, 64, 96, or 128} pixels / TDI column
TDI transfer direction	Bi-directional (“up” or “down”)
Pixel size	8.75µm x 8.75µm
Image format	107.52mm x 1.12mm
Number of output ports	8 @ Top (transfer “up”), 8 @ Bottom (transfer “down”)
Pixel rate / output (max)	20M pixel/s / output
Total pixel output rate (max)	160M pixel/s = 20M pixel/s/output x 8 outputs
Vertical (“parallel”) shift registers	3-phase
Number of isolation rows	21 top, 21 bottom (all covered by opaque light shield)
Horizontal (“serial”) shift registers	4-phase

CCD 10121 Performance Specifications					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units / Remarks**
Q_{SAT}	Saturation Charge (“Full Well”)	350	450		ke- at 12k lines/s
CG	Conversion Gain	2.5	3.3	4.0	µV/e-
V_{SAT}	Saturation Voltage		1.5		V
VLIN	Non-Linearity		1%	5%	@ 10% to 90% Full Well
DR	Dynamic Range		10,000		DR = Q_{SAT} / NE
H-CTE	Horizontal CTE	0.999985	0.999995		/transfer (4 H-transfers/pixel)
V-CTE	Vertical CTE	0.99980	0.99995		/transfer (3 V-transfers/pixel)
NE	Read Noise		40	50	e-rms
PRNU	Photoresponse Non-Uniformity		5	20	% pk-pk
F_{PIXEL}	Pixel Array Flatness		30		µm pk-pk (note 1)
DS	Dark Signal		1.3	6	nA/cm^2 at +25°C
-----	DC offset on VOUT pins		15		V
P_{AMPS}	Power dissipation: output amps		0.9		W (note 2)
$P_{H\text{-}CLK}$	Power dissipation: H-clocks		1.4		W (note 3)
$P_{V\text{-}CLK}$	Power dissipation: V-clocks		0.1		W (note 3)

Note 1: Measured to the best-fit plane to the pixel array. F_{PIXEL}<13□m pk-pk is available on special order.
Note 2: Power dissipated in R_{LOAD} resistors (which are not inside the CCD package) is not included in this total.
Note 3: Clock power dissipation is proportional to $C*V^2*f$

TEST CONDITIONS: All testing performed at:

- Temp = +25ºC typ.
- Horizontal clock frequency = 20MHz / output
- Vertical clock frequency = 12kHz
- Input voltages and load resistors R_{LOAD} at typical values, except (a) horizontal register clock offsets may be tuned as required to optimize performance, and (b) {H1, H2, H3, & H4} clock swings ≤6Vpp.
- Q_{SAT} and V_{SAT} measured in TDI-128-up and TDI-128-down modes. FF (Full-frame) mode may be used as convenient to measure other parameters.
- No binning: 1x1 full-resolution mode.



Typical QE Curve for CCD 10121

CCD HANDLING PRECAUTIONS TO PREVENT ESD DAMAGE

By their very nature, CCDs are very sensitive to electro-static discharge (ESD) damage. Special ESD-control equipment and personnel training are mandatory, particularly when installing or removing the CCD from a camera system. See Fairchild Imaging application note “Prevention of ESD Damage in CCD Image Sensors” for details. Key points:

- Use ESD-safe workbench surfaces. Cover metallic workbench surfaces with ESD-safe grounded mats. Remove non-ESD-safe materials (paper, tools with plastic handles, etc.) from work area.
- Use wrist straps or equivalent (~1MΩ to ground), ESD-safe lab coat or equivalent (buttoned—not open), and ESD-safe gloves or finger cots. Test wrist strap before handling CCDs.
- Relative humidity must be 40% min.; >50% recommended.
- Use ionizing air blowers; type: AC (not pulsed DC), balance $\leq|\pm 20V|$ max., $\leq|\pm 10V|$ recommended. Performance spec at work area: voltage decay from 1000V to 100V in <10 seconds. Measure this periodically; air ionizers require maintenance.
- Allow devices to slowly discharge in the ionized air stream when removing devices from their 1st-level container, and when removing devices from test sockets.
- The receiving socket and associated circuitry must be adequately grounded.
- Store CCDs with all pins shorted together by shorting bars, conductive foam, or the equivalent.

ESD damage invalidates the warranty.

WARRANTY AND CERTIFICATION

Within twelve months of delivery to the original customer, BAE Systems Imaging Solutions will repair or replace, at our option, any Fairchild Imaging components or camera products, if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

BAE Systems Imaging Solutions certifies that its Fairchild Imaging products are fully inspected and tested prior to shipment, and that they conform to the stated specifications.

FOR MORE INFORMATION, CONTACT

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This product is designed, manufactured, and distributed utilizing the ISO 9001:2008 Business Management System.