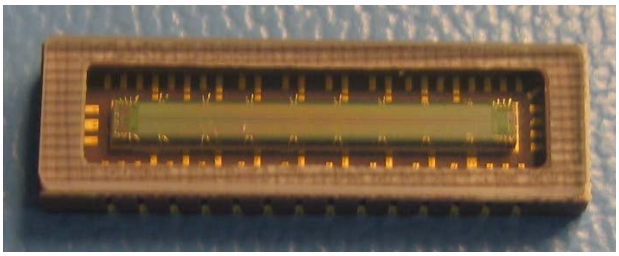
CMOS 1421
2048 x 1 Linear Image Sensor

FEATURES

- **Maximum Output Rate: 80Mpixel/sec**
- **1 or 2 Output Ports**
- **Wide Dynamic Range: 52000:1 (94dB)**
- **Excellent Linearity**
- **Low Dark Current**
- **Non-Destructive Readout for Fowler Sampling**
- **Very Low Readout Noise: 1e⁻ rms (multi-sample)**
- **Two Independent Gain Settings per Pixel**
- **Electronic Shutter and Anti-Blooming Drain**
- **3.3V 400mW Operation plus Power-Down**
- **Package Size: 22.35mm x 6.35mm x 2.85mm (l x w x h)**
- **RoHS Compliant**



APPLICATIONS

- Microscopy
- Photon Counting
- Fluorescent Imaging

DESCRIPTION

The CMOS 1421 is a high resolution 2K pixel, front illuminated linear sensor designed for scientific and medical linescan applications such as fluorescent imaging or optical inspection which require low noise, high sensitivity and wide dynamic range. The photodiode pixel has 7µm x 10µm optical area with 7µm center-to-center spacing and 85% fill factor. Several acquisition modes make operation of the sensor very flexible. *Read After Integration* mode is ideal for applications requiring high quality signals. Higher-speed *Buffered Read After Integration* mode integrates next line while reading the current. *Read On Integration,* a non-CDS mode, allows the highest speed. *Multiple Read During Integration* mode permits oversampling during integration for demanding low light applications. A JTAG-based *programmed* mode is available to meet a wide range of specialized imaging requirements. External signals control the readout cycle in this mode. Packaging options include CLCC and PLCC packages.

Pinout Diagram

(see Table 1 for pinout definitions)

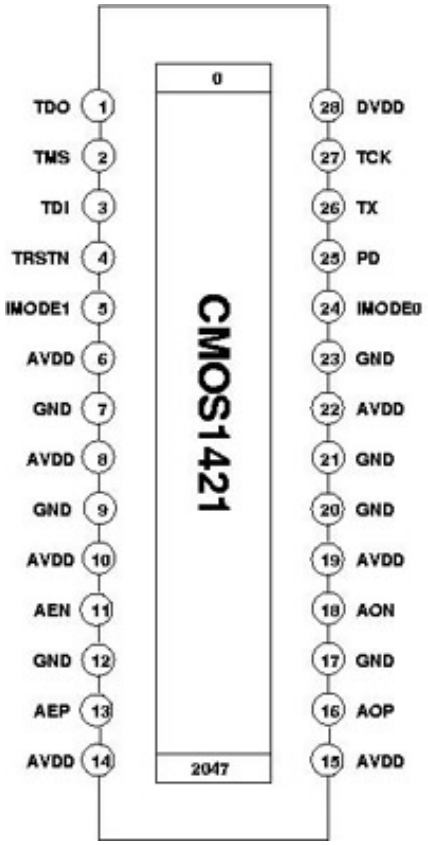


Figure 1. Block Diagram

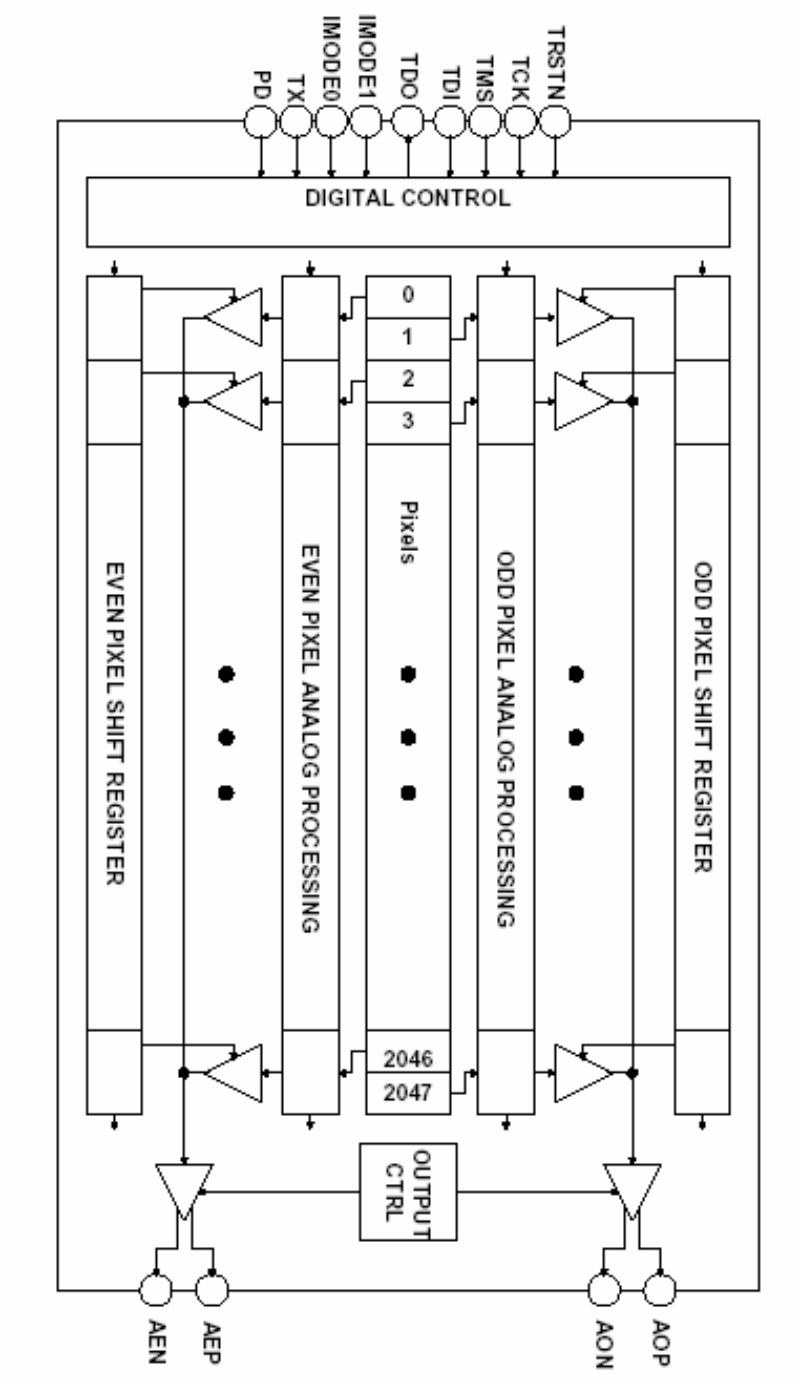


Table 1: Pin Description

Signal	Pin Number	Type	Description
Signals Used in Standard Mode			
TCK	27	Digital input	System clock providing pixel clock and JTAG clock
IMODE0	24	Digital input	Interface mode control bit 0
IMODE1	5	Digital input	Interface mode control bit 1
TRSTN	4	Digital input	System reset and JTAG reset (active low)
TX	26	Digital input	After TRSTN rises: Acquisition mode select Otherwise : Pixel reset/readout cycle
PD	25	Digital input	After TRSTN rises: Acquisition mode select Otherwise : Power-down input (active high)
TDI	3	Digital input	Data/gain shift register input or JTAG input
Output Signals			
AEN	11	Analog output	Even pixels negative analog output
AEP	13	Analog output	Even pixels positive analog output
AOP	16	Analog output	Odd pixels positive analog output
AON	18	Analog output	Odd pixels negative analog output
TDO	1	Digital output	Data/gain shift register output or JTAG output
Programmed Mode Control			
TMS	2	Digital input	JTAG mode select
Power and Ground Signals			
DVDD	28	Power	Digital power supply voltage
AVDD	6,8,10,14,15,19,22	Power	Analog power supply voltage
GND	7,9,12,17,20,21,23	Power	Ground and substrate

MODE OVERVIEW AND FEATURES

Interface Modes: The four interface modes are controlled by IMODE(0:1) inputs. The modes are single-port output, dual-port output, gain control, and JTAG control. Any of the first three of these modes may be selected for any of the acquisition modes. The fourth mode—JTAG control—determines whether the sensor will operate in *standard operation* mode or *programmed operation* mode.

In order to select the interface mode, IMODE(0:1) pins must be asserted. (See **Operation** section under **Interface Modes**.)

Acquisition Modes: The acquisition modes are set using TRSTN, TX, and PD, as described in Table 3. The acquisition modes determine how the sensor performs charge integration, reset, and readout. The key controls are:

(1) Readout during integration (overlapping of integration and readout operations), or after integration.

(2) Destructive readout (current pixel value is reset by the readout) or non-destructive (current pixel value is unaffected by the readout).

(3) Differential (full readout, including the calibration cycle required for correlated double sampling [CDS]).

A setup sequence, which may be controlled by an FPGA, is required to initialize the sensor on power up. This setup is described in **Interface Modes** section. Programmed operation mode is also described in this section. The analog output of the sensor may be single- or dual-port as determined by the interface mode. The output may also be differential or single-ended. This selection is determined by the acquisition mode.

The four acquisition modes are:

RAI (Read After Integration): After integration is completed, a pixel/calibration differential data is read out.

BRAI (Buffered Read After Integration): During integration of the current line, previous line pixel differential data is read out.

ROI (Read On Integration): During integration of the current line, previous line single ended pixel data is read out.

MRDI (Multiple Read During Integration): During integration, non-destructive, multiple readout of single ended pixel data is performed.

Figure 1 summarizes the standard operation modes that are available.

Change between the standard and programmed modes and selection of the acquisition modes require a reset sequence. The other modes can be changed during sensor operation. The acquisition and interface modes are described in detail in the **Operation** section.

OPERATION

The operation of the pixel array contained in CMOS 1421 is shown in Figure 2. Each pixel has a photodiode, a pixel amplifier, and a sample and hold circuit. Each pixel also contains one bit of the gain register and noise suppression circuitry which are not shown in Figure 2. The S1 and S2 signals shown in the figure are internally generated depending on the selected acquisition mode. The amplifiers and other pixel circuitry are organized into two halves, even (lower) and odd (upper), as shown in the block diagram.

Pixel transfer and/or reset is initiated when TX is pulsed for one clock cycle. All input signals are sampled on the rising edge of TCK. When a single-clock-cycle pulse is applied to TDI, it is serially shifted, on the rising edge of each TCK, through a 2052-bit pixel output enable shift register. The first two and last two bits are dummy pixels and the middle 2048 bits each act as an enable for the shift register bit's respective pixel output buffer. The output buffers are multiplexed onto the AEP and AEN pins, and/or the AOP and AON pins, depending on the interface mode. The pixel output enable shift register is clocked on the rising edge of TCK.

Figure 2: Summary of Standard Configurations

The User Chooses Any of Four Pixel Readout Modes			The User Chooses Either of Two Output Modes			
Readout Mode Name	What It Is	Output Signal Type	Single-Port Output Mode "Even" port is used. "Odd" port is not used		Dual-Port Output Mode Both "Even" and "Odd" ports are used	
RAI Single Destructive Readout Readout Occurs After Integration, Before the Next Integration Cycle Can Begin	Readout does not start until integration is complete. Integration does not resume until readout is complete. On-chip control circuitry is off during pixel integration so as to minimize noise picked up by the pixels. RAI is slower than some of the other modes because integration and readout occur sequentially rather than simultaneously.	Differential Output Signal A calibration circuit for external correlated double sampling (CDS) is enabled	Pixel data available 25nSec after rising edge of each clock cycle. External CDS calibration data available 25nSec after falling edge of clock. 20MHz maximum data output rate. The maximum data rate is determined by the sum of these two 25nSec analog output delays above.	*this is config* ***1*** *RAI single output port*	On the Even port, data for Pixel "N" becomes available 25nSec after the falling edge of every second clock cycle. Calibration data for that pixel becomes available 25nSec after the falling edge of the next clock cycle. On the Odd port, data for Pixel "N+1" becomes available one clock cycle after data for Pixel "N" became available in the Even port. 40MHz maximum data output rate. The maximum data rate is determined by one analog output delay as opposed to two analog output delays for the single-output-port case to the left.	*this is config* ***2*** *RAI dual output port*
BRAI Single Destructive Readout Readout of an Integration Occurs During Next Integration Cycle	While a line is being integrated, the previous line can be read out. No calibration data is presented, increasing readout rate by two fold. Output is still two-sided, enabling correlated double sampling and reduction of fixed pattern noise.	Two-sided Output Signal Positive analog output contains pixel reset value. Negative output is integrated value.	Pixel data available 25nSec after rising edge of each clock cycle. 40MHz maximum data output rate. The maximum data rate is determined by one analog output delay. This is twice the speed of RAI mode because there is no time spent presenting calibration data.	*this is config* ***3*** *BRAI single output port*	Pixel data becomes available on the Even output port 25nSec after the falling edge of each clock cycle. Pixel data for the following line becomes available on Odd port 25nSec after the falling edge of the next clock cycle. 80MHz maximum data output rate.	*this is config* ***4*** *BRAI dual output port*
ROI Single Destructive Readout Readout of an Integration Occurs During the Next Integration Cycle	This produces a single-ended-output. Faster operation is achieved than is possible with RAI, because the calibration circuit is disabled so as to devote internal circuitry solely to rapidly clocking out data. Read noise & fixed pattern noise are degraded as compared to RAI.	Single-Ended Output Signal The calibration circuit for external CDS is disabled	Pixel data becomes available 25nSec after the rising edge of each clock cycle There is no CDS calibration signal in single-ended output format	*this is config* ***5*** *ROI single output port*	Pixel data becomes available on the Even output port 25nSec after the falling edge of each clock cycle. Pixel data for the following line becomes available on Odd port 25nSec after the falling edge of the next clock cycle.	*this is config* ***6*** *ROI dual output port*
MRDI Multiple Non-Destructive Readouts Readouts are performed while the pixel is integrating	Pixels can be sampled multiple times during integration. Read Noise and Fixed Pattern Noise can be averaged and further suppressed as compared to the other modes. Read noise as low as 1 electron is achievable with high pixel gain setting and 16X oversampling.		40 MHz maximum data output rate. The maximum data rate is determined by one analog output delay. This is twice the speed of the differential-output modes above running on a single output port. This is because there is no need to fit in the calibration data.	*this is config* ***7*** *MRDI single output port*	There is no CDS calibration signal in single-ended output format. 80MHz maximum data output rate.	*this is config* ***8*** *MRDI dual output port*

Acquisition Modes

The pixel circuits can be operated in four different data acquisition modes: RAI, BRAI, MRDI, and ROI. These modes select between different speed/noise tradeoffs to support a wide range of applications. In each mode, TX and TDI control sequencing.

The acquisition modes are selected by sampling the TX and PD plus (see Table 3) on the first rising edge of TCK after TRSTN rises. Note that the normal functions of TX and PD are suppressed after TRSTN falls until one clock after TRSTN rises; i.e. after they have been sampled to determine the acquisition mode.

RAI—Readout After Integration (see Figure 5): Differential pixel data is available for destructive readout (current pixel value is destroyed by readout) after photocharge integration is complete. This is the simplest mode. TX starts and ends pixel reset and starts integration and TDI ends integration and starts pixel readout. Fixed pattern noise (FPN) may be removed by performing external chip level CDS on the pixel and calibration data. Therefore, each pixel value can be determined by calculating

$$S_{out} = (AEP_p – AEN_p) – (AEP_c – AEN_c),$$

where AEP_p and AEN_p are the pixel values on AEP and AEN respectively, and AEP_c and AEN_c are the calibration values on AEP and AEN respectively. In dual-port output mode, the odd pixel data will appear on AOP and AON instead. Additional information about RAI mode is shown in Figures 5, 10, 13 and the timing equations are given in **Integration Time and Line Rate Calculations** section.

BRAI—Buffered Read After Integration (see Figure 6). Differential pixel data from the previous line is available for destructive readout while the current line is integrating. BRAI mode is faster than RAI mode since calibration data is not presented and pixel data from the previous line is buffered for readout while the sensor is integrating the current line. TX starts and ends pixel reset, and starts a new integration. TDI ends integration, buffers the captured data, and starts pixel readout of the buffer. Another TX may begin immediately after TDI so that reset and integration can proceed during readout of the buffered values.

As with the RAI acquisition mode, the fixed pattern noise (FPN) in the differential output path can be removed by performing external chip level CDS on the pixel data. Since there is no calibration data in BRAI mode, the calculated value is simply

$$S_{out} = (AEP_p – AEN_p)$$

Substitute AOP and AON in the above for odd pixel data in dual-port output mode.

ROI—Readout On Integration (see Figure 7). Single-ended pixel data from the previously-scanned line is available on one of the differential output pins while the current scan line data is being integrated. ROI mode produces the highest line scan rate, sacrificing FPM and read noise. Similar to BRAI, ROI mode allows for a single read of each pixel after each integration period. The difference is in the operation of the pixel and output circuitry. In ROI mode, the CDS circuit is disabled and analog pixel data is single-ended. AEP should be shorted to AEN, and AOP should be shorted to AON, since pixel data toggles between the two every line. TX ends integration, captures the integrated data, starts and ends pixel reset, and starts a new integration, and TDI starts pixel readout of the previously-captured data.

MRDI—Multiple Readout During Integration (see Figure 8). Single-ended pixel data can be read out multiple times during photocharge integration. MRDI mode provides the lowest noise through the use of oversampling. This mode is intended for applications that require very low read noise. Since the readout is non-destructive, each pixel can be read out multiple times and averaging/oversampling techniques such as Fowler sampling can be applied to effectively reduce the readout noise. TX starts and ends pixel reset and starts integration, and TDI starts pixel readout.

In MRDI and ROI acquisition modes, no calibration data is generated. Therefore, data is

read out single-ended and is available during the entire pixel readout cycle. This allows the sensor to be read out twice as fast as RAI and BRAI acquisition modes.

Programmed Mode (see Figure 9). Data acquisition is performed using the sensor input pins only; i.e., no internal counters are used. Setup for this mode is discussed in **Interface Modes** section. Figure 9 shows how to control RAI and MRDI acquisition modes in terms of the internal signals. For additional information about programmed mode operation using other acquisition modes, please contact Fairchild Imaging technical support.

Pixel-Level Gain Control

Each pixel amplifier has bi-level digitally programmable gain and an anti-blooming drain. The pixel-level gain affects sensitivity, conversion factor and noise of the sensor. The gain of each pixel amplifier is set by shifting in a string of 2052 bits into the pixel gain register using clock (TCK) and data input (TDI) while the interface mode pins select the GAIN control (IMODE[0:1] = 11). As in the pixel data enable shift register, the first two and last two bits in the gain shift register are for dummy pixels. High gain is selected with a logical low, and low gain is selected with a logical high. The initial condition of each bit in the gain register is logical low; i.e. high gain.

Digital Timing

Timing diagrams for the digital inputs and outputs are given in Figures 16 and 17, and the corresponding timing data are in Tables 11 and 12. Note that timing values are different for single-port and dual-port output modes. When PD is high, the chip goes into power-down mode to conserve power while the sensor is not in use. When TRSTN is low, the sensor's internal registers are set to zero, and all of the digital inputs are disabled including PD. If the sensor is not reset after power-up, TRSTN must be pulsed low during the power-up cycle for the sensor to operate correctly.

Interface Modes

The CMOS 1421 can be operated in four different interface modes: single-port output, dual-port output, gain register control and JTAG programming. JTAG programming is presently supported only for use of programmed mode. These interface modes are controlled by pins IMODE0 and IMODE1 as described in Table 4. Interface modes are determined by sampling the IMODE0 and IMODE1 pins during the rising edge of TCK. Of the four possible combinations, two are used to access the pixel data enable shift register and thus send pixel data to the AEP and AEN and/or AOP and AON pins, one is to access the pixel gain register, and the last allows JTAG access to internal timing and operation registers.

In single-port output mode (IMODE[0:1] = 10), all pixel data is read from the AEP and AEN analog output port. In dual-port output mode, data from odd and even pixels are read from two output ports. AEP and AEN generate even pixel data, and AOP and AON generate odd pixel data. Dual-port output mode achieves twice the pixel throughput of the single-port output mode if the output ports are at their maximum bandwidth, which is achieved for the TCK frequencies shown in Table 5. While in either dual-port or single-port output mode, readout of the sensor is always initiated by pulsing TDI for one clock cycle. During each clock cycle one pixel is read out. The first two and last two pixels in the 2052 bit pixel data enable shift register are dummy pixels. In dual-port output mode (IMODE[0:1[= 01), both analog output ports are active for 2052 clock cycles.

Pixel timing for single-port output mode in both RAI/BRAI and MRDI/ROI acquisition modes is shown in Figures 10 and 11. Figure 12 shows the position of TDI and TDO with respect to the first and last pixels in single-port output mode. Pixel timing for dual-port output mode in both RAI/BRAI and MRDI/ROI acquisition modes is shown in Figures 13 and 14. Figure 15 shows the position of TDI and TDO with respect to the first and last pixels in dual-port output mode. In single-port output mode (IMODE[0:1] = 01), only

the even pixel output port is active for 2052 clock cycles.

In order to use programmed mode, an initialization sequence must be transmitted through the JTAG interface. This is done by setting IMODE[0:1] = 00 and clocking in the data sequence in Table 2. Note that the rising edge of TCK is used to clock data in. The entries in Table 2 labeled 12, 11, and 10 are set to 0,1,0 for dual-port output and 0,0,1 for single-port output mode. Reset and integration are controlled by setting the appropriate counter register values for the internal control signals (see CMOS 1421 JTAG application note). The sensor is read out by setting TX low and pulsing TDI high for two clock cycles. After readout, programmed mode can be resumed by setting TX high for one clock cycle.

Table 2: Programmed Mode (JTAG) Startup Sequence

TMS	1	1	1	1	1	0	1	1	0	0	0	0	1	1	1	0	0	0
TDI	0	0	0	0	0	0	0	0	0	0	10	11	12	0	0	0	0	0
TX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Tables 3 and 4 summarize how to enter specific acquisition or interface modes, and Table 5 shows the maximum pixel clock frequency in various acquisition/interface modes.

Table 3: Acquisition Modes

PD:TX	Mode
00	RAI
01	ROI
10	MRDI
11	BRAI

Table 4: Interface Modes

IMODE0:1	Mode
00	JTAG access
10	Single-port output
01	Dual-port output
11	Gain register access

Table 5: Maximum TCK Frequency

Interface/Acquisition Mode	Frequency
Single-port RAI	20 MHz
Single-port BRAI or MRDI	40 MHz
Single-port ROI	50 MHz
Dual-port RAI	40 MHZ
Dual-port BRAI or MRDI	80 MHz
Dual-port ROI	100 MHz

Electrical and Optical Characteristics

Table 6: Absolute Maximum Ratings

Parameter	Min	Nom	Max	Units
Power supply voltage			4.0	V
Input voltage	-0.4		V_{DD} + 0.4	V
Output voltage	-0.4		V_{DD} + 0.4	V
Storage temperature	-60		125	ºC
ESD tolerance	2000			V

Table 7: Operating Conditions

Parameter	Min	Nom	Max	Units
Power supply voltage (V_{DD})	3.0	3.3	3.6	V
Digital high input voltage (V_{IH})	V_{DD} – 0.7		V_{DD} + 0.4	V
Digital low input voltage (V_{IL})	0		0.7	V
Digital high output voltage (V_{OH}) with I_{OH} = -1mA	2.1			V
Digital low output voltage (V_{OH}) with I_{OL} = 1mA			0.4	V
Temperature (T_A)	-60	0	40	ºC

Note 1. All voltages are referenced to GND.
Note 2. The human body model is used for ESD testing (1.5kΩ resistor in series with a 100pF capacitor).

Table 8: Electrical Specifications CMOS 1421, V_{DD} = 3.3V, T = 25ºC

Parameter	Min	Nom	Max	Units
Pixel count		2048		
Pixel size		7 x 7		μm^2
Fill factor		85		%
Supply current per active output		25	30	mA
Supply current (outputs inactive during integration)		45	60	mA
Supply current (power down)		10	20	µA
Output capacitive load	35	40	45	pF
Output resistive load	1	2.2	10	kΩ
RIR	99.75			%
RIL			0.25	%
Nonlinearity			1	%
Logic clock	0.1		100	MHz
Non-functional pixels			5	

Table 9: RAI Acquisition Electrical Specifications CMOS 1421, T_{int} = 5ms, V_{DD} = 3.3V, T = 25ºC

Parameter	Min	Nom	Max	Units
Output swing	1.0		1.5	volts
Sensitivity (high gain)		25 169		V/lux-sec V/µJ/cm^2
Sensitivity (low gain)		2.5 16.9		V/lux-sec V/µJ/cm^2
Pixel response nonuniformity			±5	%
Pixel differential nonuniformity			±2.5	%
Dark signal nonuniformity			5	mV
Dark signal response			5	mV
Conversion gain (high gain)		270		µV/electron
Conversion gain (low gain)		27		µV/electron
Usable full well capacity (high gain)		5200		electrons
Usable full well capacity (low gain)		52000		electrons
Saturation exposure (high gain)		60 9		mlux-sec nJ/cm^2
Saturation exposure (low gain)		607 90		mlux-sec nJ/cm^2

Table 10: Speed/Noise Electrical Specifications CMOS 1421, T_{int} = 100µs, V_{DD} = 3.3V, T = 25

Parameter	RAI	BRAI	MRDI	ROI	Units
Pixel rate per port	20.0	40.0	40.0	50.0	MHz
Dark current	12.0				e-/pixel/msec
Read noise (high gain)	3	5	1 *	12	electrons
Read noise (low gain)	10				electrons
Noise equivalent exposure (high gain)	46 6.6	46 6.6	11.6 * 1.7 *		µlux-sec pJ/cm^2
Noise equivalent (low gain)	116 16.6	116 16.6			µlux-sec pJ/cm^2
Dynamic range			52000 94		dB

* 16x oversampling

Image Lag Specification

A diagram of the measurement of the residual image (RIL and RIR) specifications from Table 8 are shown in Figure 3.

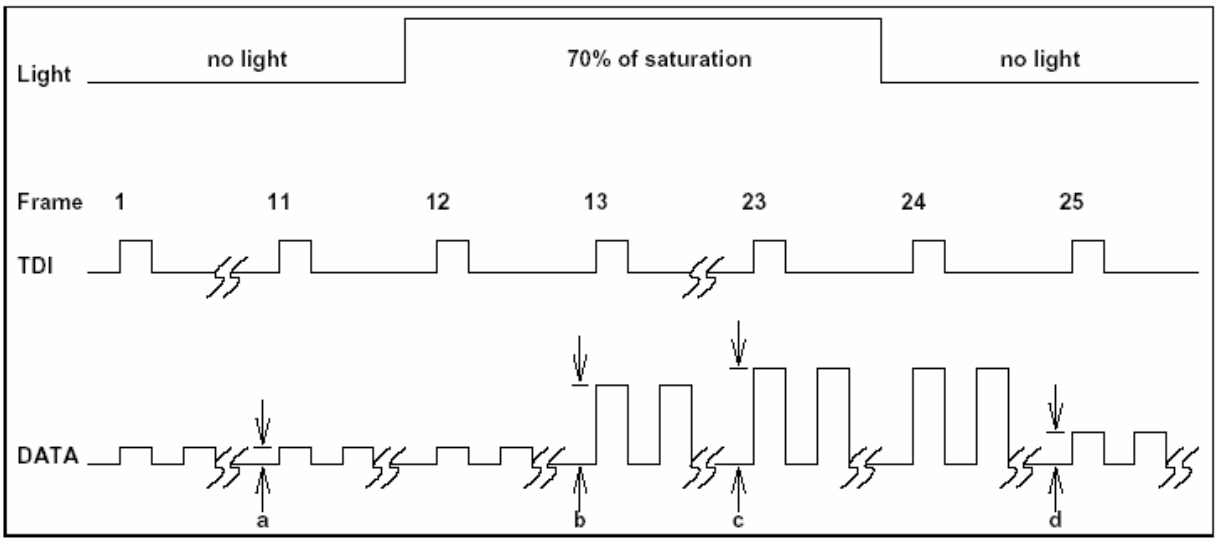


Figure 3: RIL and RIR definitions assuming CLK=10MHz, T_{int}=5ms, and RAI mode

Quantum Efficiency

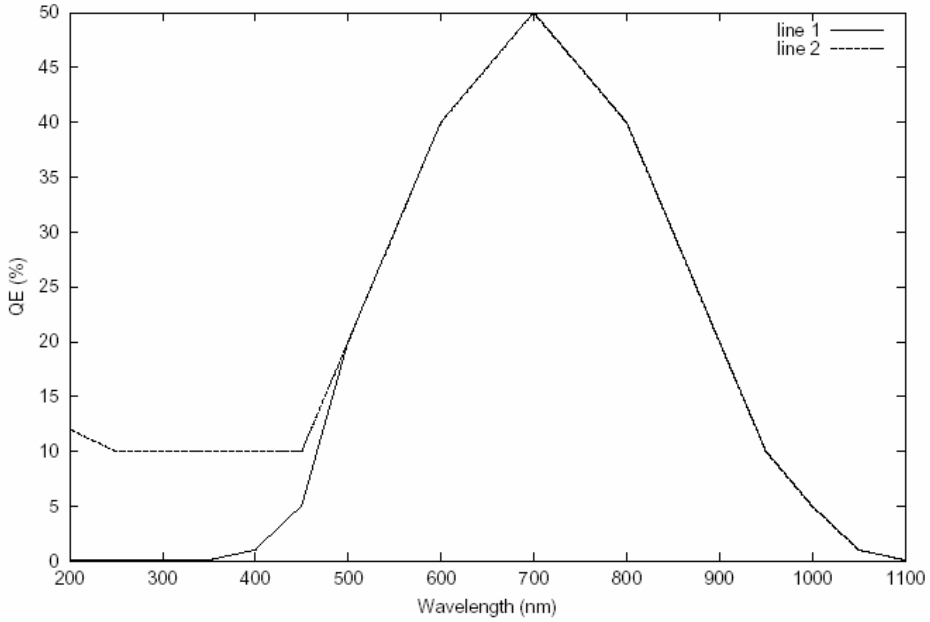


Figure 4: Quantum Efficiency

Note 1. 100% fill factor is assumed when quantum efficiency is estimated.

DEFINITIONS

1 lux-s = 146.41nJ/cm^2 at 555nm.

Conversion gain: The gain from the pixel to the output of the sensor.

Dark current: The photodiode current under dark conditions.

Dark signal nonuniformity: The RMS signal variation S_{out} under dark conditions.

Dark signal response: The average S_{out} under dark conditions.

Destructive / non-destructive readout: Destructive readout destroys the current pixel value during readout, but non-destructive readout leaves the pixel value unaffected. Using non-destructive readout permits repeated sampling during integration.

Dynamic range: Defined as the full well capacity divided by the input referred read noise, or equivalently the output swing divided by the output referred read noise.

Fill factor: The effective percentage of the pixel area occupied by the photodiode. Pixel area is defined as the pixel pitch times the height of the light-exposed diode area.

Fixed pattern noise (FPN): The difference between the average values of individual pixels under equal illumination. Note that FPN is not noise. It is the deterministic offset due to physical differences between pixels. Correlated double sampling (CDS) is commonly used to remove FPN.

Full well capacity: The maximum number of electrons the pixel can collect before S_{out} saturates. Equivalently, the output swing divided by the conversion gain.

Logic clock: The external clock (TCK) rate for operating the digital logic, assuming a 50% duty cycle.

Nonlinearity: Measured between 0% (dark) and 70% (light) of saturation. Given a set of S_{out} measurements for light levels within this range, nonlinearity is defined as the maximum S_{out} deviation from a linear least squares fit to these measurements. The result is expressed as a percentage of S_{out} at 70% of saturation.

Noise equivalent exposure: The input energy required to produce a change in S_{out} equal to the RMS read noise of the sensor.

Output swing: The difference between the minimum and maximum S_{out}.

Pixel rate: The rate for transmitting analog pixel data out of the chip. The clock is TCK, but the pixel rate is determined by TCK and the port setting (single or dual). In dual port mode the pixel rate at each channel is half the clock rate since a pixel value is sampled from one port on even clock cycles and the other port on odd clock cycles. Note that a valid analog output must settle to within 0.25% of the final value at the end of a read cycle.

Pixel count: The number of pixels in the pixel array.

Pixel differential nonuniformity: The maximum pixel to pixel difference defined by

$$D_v = \max_i \left| \frac{S_{out\,i} - S_{out\,i+1}}{S_{out\,i} + S_{out\,i+1}} \right|$$

The measurement is done at 70% of saturation.

Pixel response nonuniformity: The maximum difference between S_{out} from any single pixel and the average S_{out} from all the pixels. The measurement is done at 70% saturation.

PSRR (0-10kHz): The power supply rejection ratio referenced to the pixel from 0Hz to 10kHz,

$$PSRR = \left(\frac{S_{out} / V_{pixel}}{S_{out} / \tilde{V}} \right)$$

where V_{pixel} is the input signal at the pixel and $\tilde{V}$ is the ripple on the power supply.

Read noise: The RMS input referred noise with zero integration time at 10Mpixels/sec.

RIL: The rate of image lag $\frac{d-a}{c-a}$ shown in Figure 3. This is the ratio of an unilluminated pixel's

response when first unilluminated to when it has been illuminated for at least 10 exposures.

RIR: The rate of image response $\frac{b-a}{c-a}$ shown in Figure 3. This is the ratio of an illuminated pixel's response when first illuminated to when it has been illuminated for at least 10 exposures.

Sensitivity: The change in S_{out} per unit change in incident radiation.

Saturation exposure: the incident radiation necessary to saturate S_{out}.

$$S_{out} = (AEP_p – AEN_p) – (AEP_c – AEN_c)$$

for RAI, destructive differential mode, and

$$S_{out} = (AEP_p – AEN_p)$$

for BRAI mode.

TIMING PARAMETERS AND WAFEFORMS

This section provides the timing parameters, waveforms, and timing equations required for operation. The timing equations are given in **Integration Time and Line Rate Calculations** section.

Signals which are in time units use the letter T. Signals in logic clock units use N. The term "clocks" in the tables always means logic clock. The signal T_{TCK} is the clock period of the logic clock.

Table 11: Single-port Output Timing Parameters with V_{DD} = 3.3V, T_A = 25ºC, and DOUT load of 10pF

Parameter	Definition	Min	Nom	Max	Units
T_1	Setup time for TDI and TX	10			ns
T_2	Hold time for TDI and TX	10			ns
T_3	Rise or fall time for TCK		*	25	ns
T_4	TRSTN pulse width	2			µs
T_5	CLK rising to TMS falling after TRSTN rising	10			ns
T_6	TRSTN falling to TX/PD changing	0			ns
T_7	TX pulse width	20			ns
N_8	Reset period in RAI mode	400			clocks
N_9	TX rising to TDI rising in RAI mode	401			clocks
N_{10}	Reset period in MRDI mode	200			clocks
N_{11}	TX rising to TDI rising in MRDI mode	201			clocks
N_{12}	Reset period in BRAI mode	600			clocks
N_{13}	TX rising to TDI rising in BRAI mode	601			clocks
N_{14}	Reset period in ROI mode	250			clocks
N_{15}	TX rising to TDI rising in ROI mode	0		0	clocks
T_{16}	TCK falling to TDO rising			10	ns
T_{17}	TCK falling to TDO falling			10	ns
T_{18}	TCK high in RAI mode	25			ns
T_{19}	TCK period in RAI mode	50			ns
T_{20}	TCK high in BRAI, ROI, and MRDI modes	12.5			ns
T_{21}	TCK period in BRAI, ROI, and MRDI modes	25			ns
T_{22}	Analog output delay			25	ns

* 10% of TCK period recommended.

Table 12: Dual-port Output Timing Parameters with V_{DD} = 3.3V, T_A = 25ºC, an DOUT load of 10pF

Parameter	Definition	Min	Nom	Max	Units
T_1	Setup time for TDI and TX	10			ns
T_2	Hold time for TDI and TX	10			ns
T_3	Rise of fall time for TCK		*	25	ns
T_4	TRSTN pulse width	2			µs
T_5	CLK rising to TMS falling after TRSTN rising	10			ns
T_6	TRSTN falling to TX/PD changing	0			ns
T_7	TX pulse width	20			ns
N_8	Reset period in RAI mode	800			Clocks
N_9	TX rising to TDI rising in RAI mode	801			Clocks
N_{10}	Reset period in MRDI mode	400			Clocks
N_{11}	TX rising to TDI rising in MRDI mode	401			Clocks
N_{12}	Reset period in BRAI mode	1200			Clocks
N_{13}	TX rising to TDI rising in BRAI mode	1201			Clocks
N_{14}	Reset period in ROI mode	500			Clocks
N_{15}	TX rising to TDI rising in ROI mode	0		0	Clocks
T_{16}	TCK falling to TDO rising			10	ns
T_{17}	TCK falling to TDO falling			10	ns
T_{18}	TCK high in RAI mode	12.5			ns
T_{19}	TCK period in RAI mode	25			ns
T_{20}	TCK high in BRAI, ROI, and MRDI modes	6.25			ns
T_{21}	TCK period in BRAI, ROI, and MRDI modes	12.5			ns
T_{22}	Analog output delay			25	ns

* 10% of TCK period recommended.

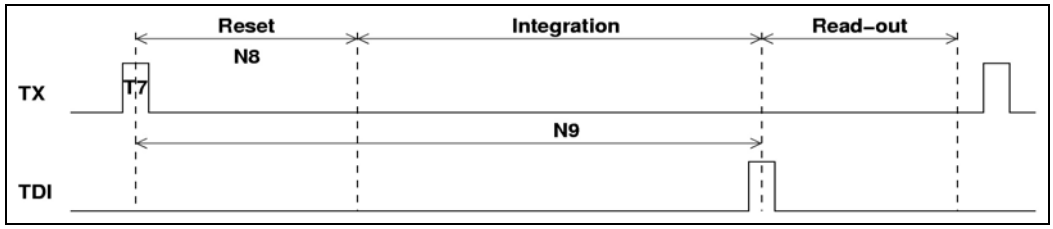


Figure 5: Timing Diagram: RAI mode

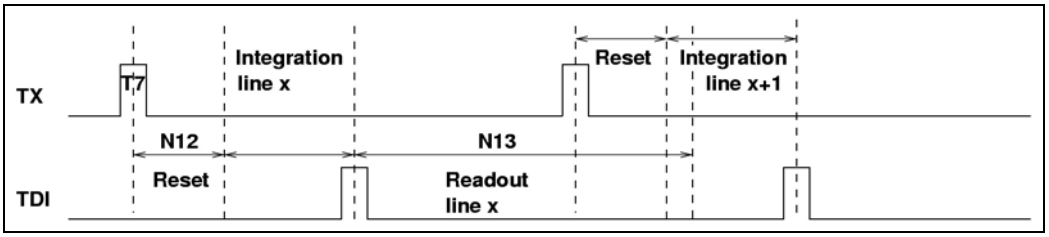


Figure 6: Timing Diagram: BRAI mode

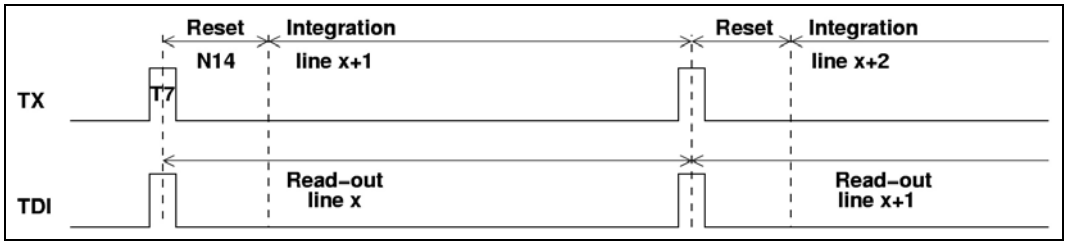


Figure 7. Timing Diagram: ROI mode

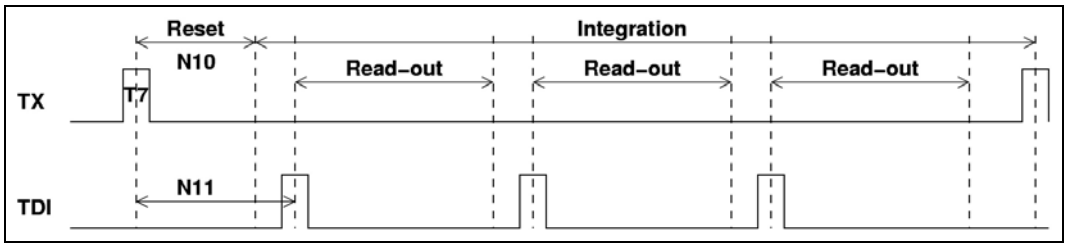


Figure 8: Timing Diagram: MRDI mode

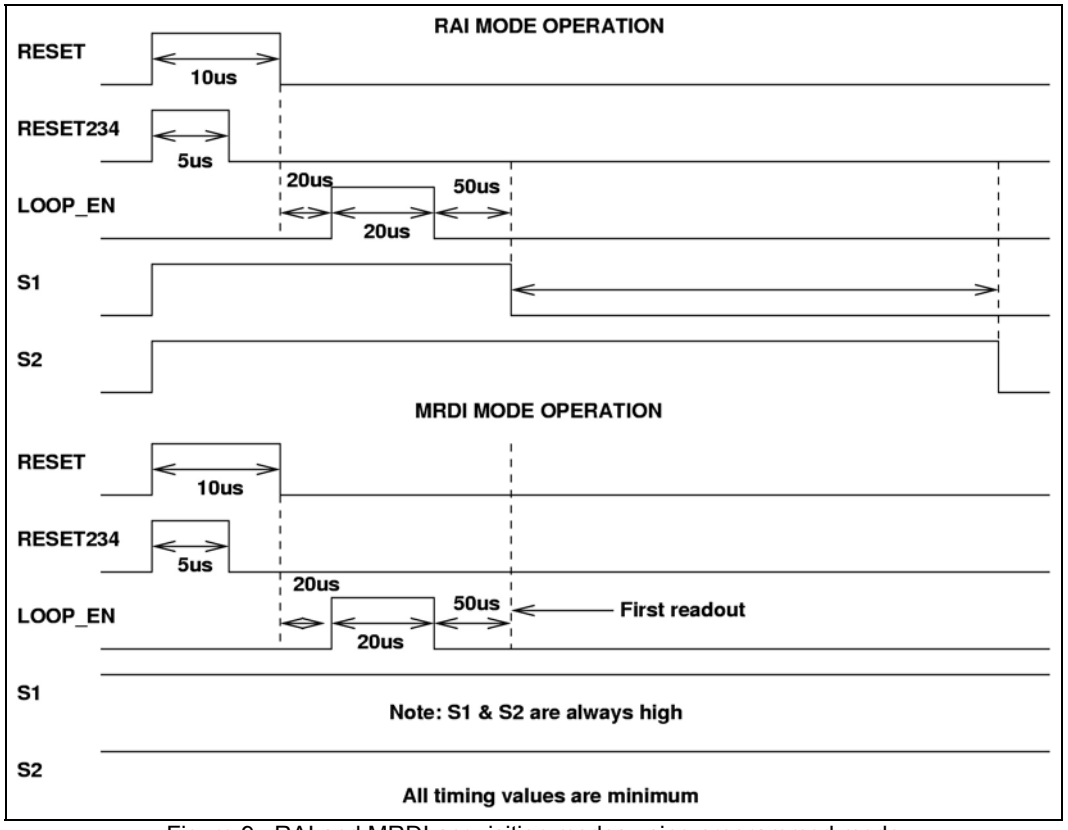


Figure 9: RAI and MRDI acquisition modes using programmed mode

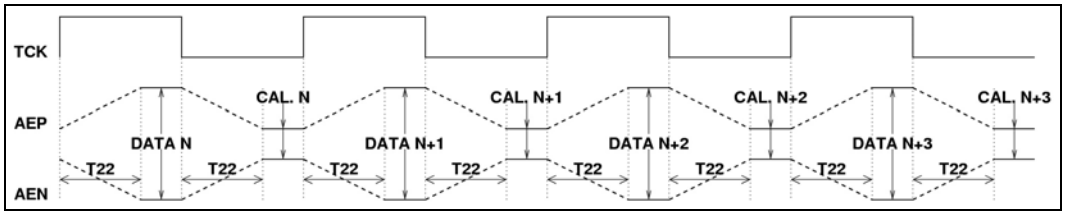


Figure 10: Single-port output: analog output waveform in RAI mode

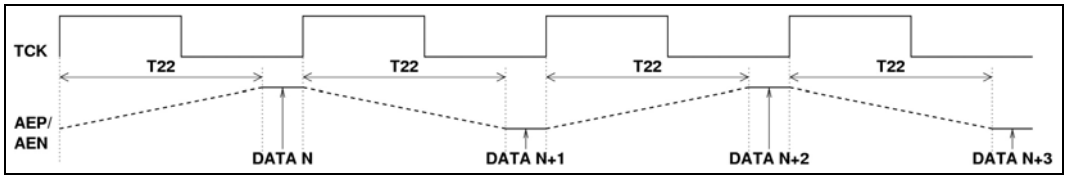


Figure 11: Single-port output: analog output waveforms in MRDI and ROI modes

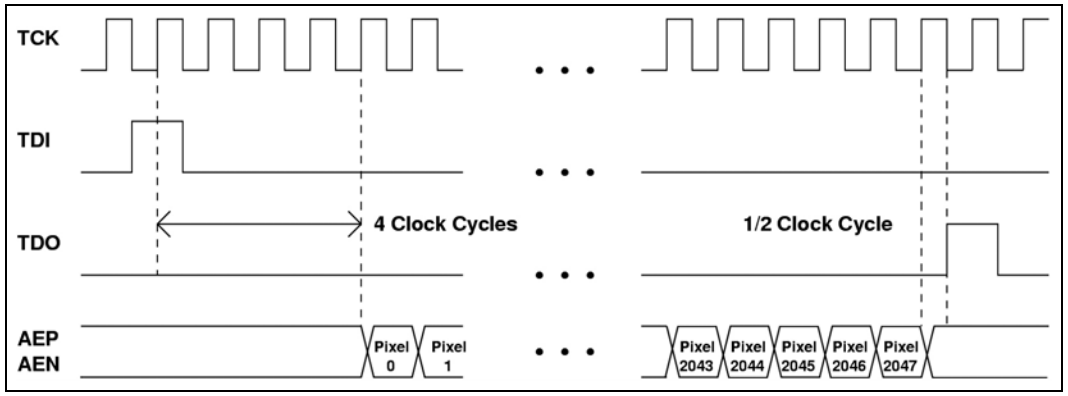


Figure 12: Single-port output: pixel positions relative to TDI and TDO

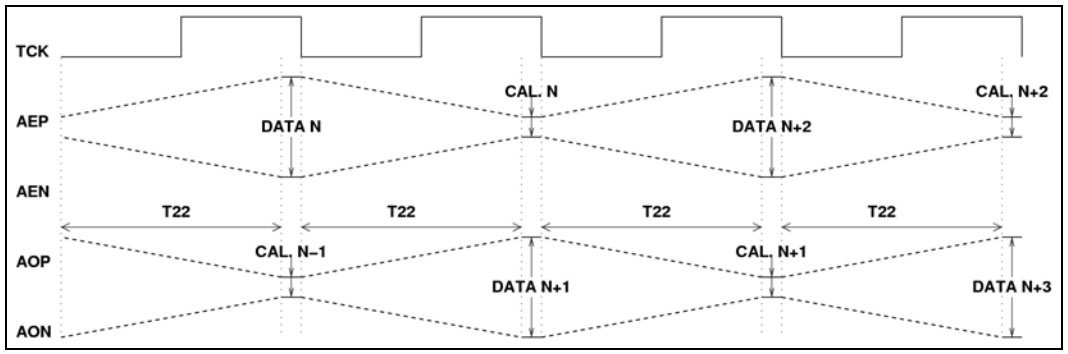


Figure 13: Dual-port Output: analog output waveform in RAI mode

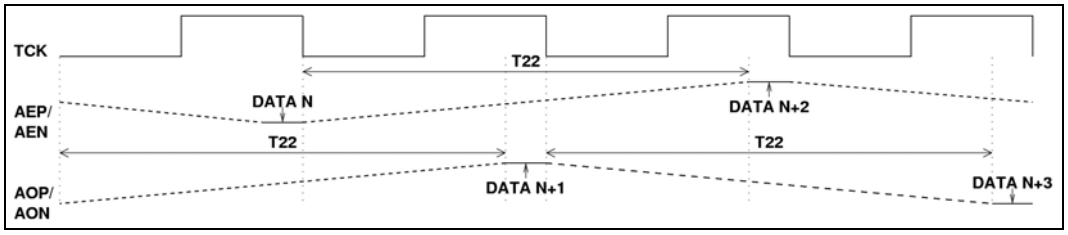


Figure 14: Dual-port Output: analog output waveforms in MRDI and ROI modes

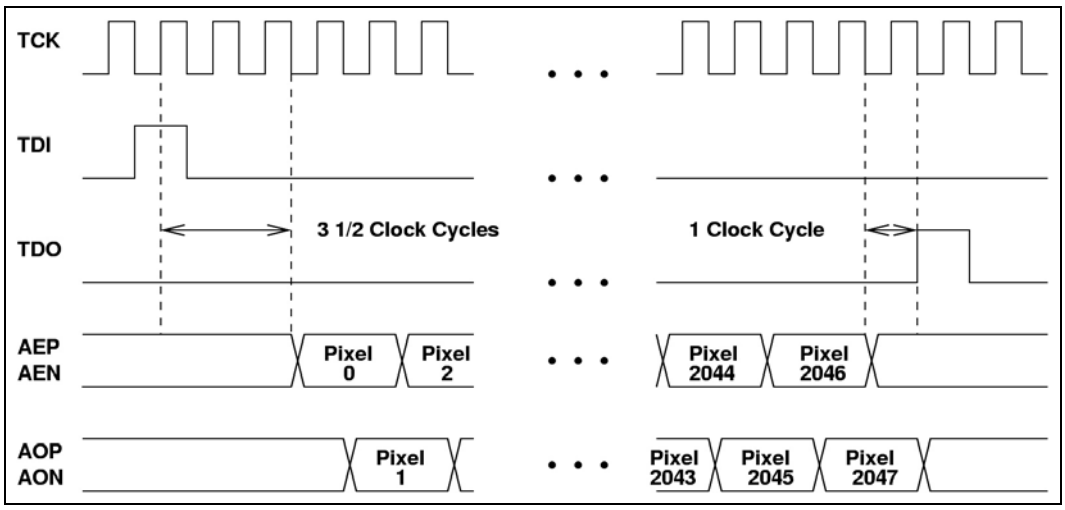


Figure 15: Dual-port Output: pixel positions relative to TDI and TDO

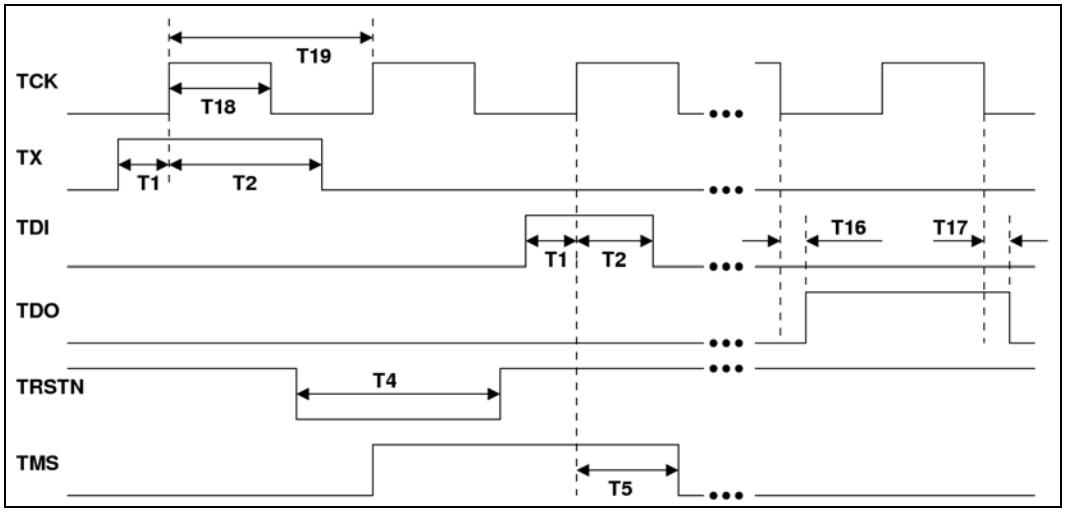


Figure 16: Digital I/O timing waveforms

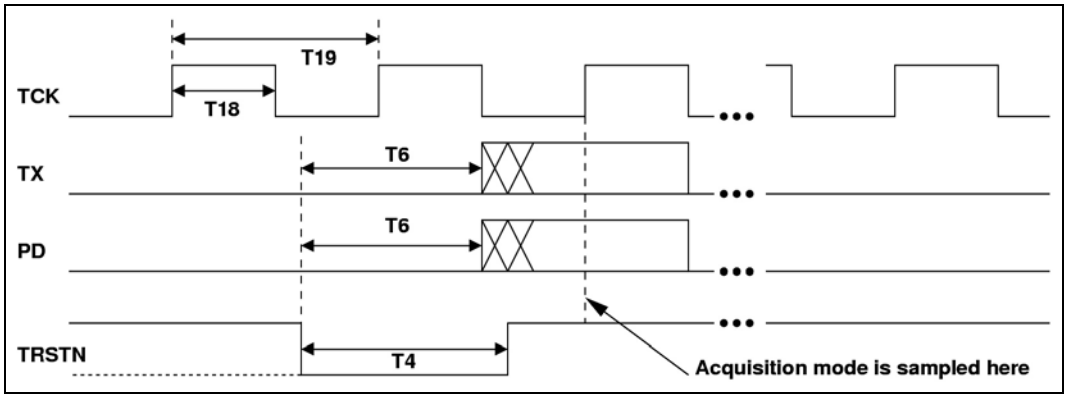


Figure 17: Power up and digital reset timing waveforms

Integration Time and Line Rate Calculations

The integration time in logic clocks, N_{int}, is calculated from the timing of TX and TDI differently for each acquisition mode. Consequently. The line rate R is different for each mode as well.

To simplify the calculations below, we will define the following terms:

$N_{TX \rightarrow TDI}$	=	logic clock periods from TX to TDI
$N_{readout}$	=	logic clock periods from TDI to TDO
$N_{TDI \rightarrow TX}$	=	logic clock periods from TDI to next TX
$N_{TX \rightarrow TX}$	=	logic clock periods from one TX pulse to the next

Note that $N_{readout}$ is always 2052. R is in Hertz and all "N" variables are in logic clock cycles. f_{TCK} is the logic clock frequency. In all modes, the maximum for R is reached as $N_{int} \rightarrow 0$.

- RAI
  - $N_{\text{int}} = N_{TX \rightarrow TDI} - N_8$

    Photocharge integration begins N_8 after TX, and ends at the next TDI.
  - $R \leq \dfrac{f_{TCK}}{N_8 + N_{\text{int}} + N_{readout}}$; equality occurs when $N_{TDI \rightarrow TX} > N_{readout}$.
  - Require $N_{TX \rightarrow TDI} > N_8$, $N_{TDI \rightarrow TX} > N_{readout}$, and $N_{TX \rightarrow TX} > N_8 + N_{readout}$.
  - See Figure 5.

- BRAI
  - $N_{\text{int}} = N_{TX \to TDI} - N_{12}$

    Photocharge integration begins N_{12} after TX and ends at the next TDI.
  - $R \le \dfrac{f_{TCK}}{\max\left(N_{12} + N_{\text{int}}, N_{readout}\right)}$.
  - Require $N_{TX \to TDI} > N_{12}$, $N_{TDI \to TX} > 0$, and $N_{TX \to TX} > \max\left(N_{12}, N_{readout}\right)$.
  - See Figure 6.

- ROI
  - $N_{\text{int}} = N_{TX \to TX} - N_{14}$.
  - Photocharge integration begins N_{14} after TX and ends at the next TX.
  - $R = \dfrac{f_{TCK}}{N_{14} + N_{\text{int}}}$
  - Require $N_{TX \to TDI} = 0$ and $N_{TX \to TX} > \max\left(N_{14}, N_{read-out}\right)$.
  - See Figure 7.

QUESTIONS AND ANSWERS

When should I use programmed mode:

A prominent case where programmed mode is advantageous is if the logic clock (TCK) must be much slower than the maximum clock speed. For example, if the sensor is operated with 1MHz clock, instead of a 20MHz clock, programmed mode can be used to significantly reduce the reset period of the sensor.

In RAI acquisition mode, why does the sensor's output read zero when the input illumination is increased sufficiently above saturation?

In RAI acquisition mode, the CMOS 1421 double-samples the pixel-level amplifier, once after reset and once after integration is complete. If the illumination is high enough, both the sample after reset and the sample after integration will be the same, causing the output to be zero.

Under dark conditions the first 50-100 pixels are saturated. How can this problem be corrected?

Typically, this problem is caused by undershoot of the digital input pads. When the voltage on one of the digital input pads falls below ground, the sensor ESD protection diode turns on and current is injected into the substrate. The CMOS 1421 can "see" this substrate current. We recommend using 330Ω resistors in series with the digital input signals. This typically corrects the problem; if not, try slightly larger series resistors.

How do I process the pixel data collected in MRDI acquisition mode to reduce read noise?

See J.D. Garnet and W.J. Forrest, "Multiply-sampled read-limited and background-limited noise performance," in Proceedings of SPIE, Vol. 1946, 1993, pp. 395-404.

PACKAGES

The CMOS 1421 package is a ceramic (low temperature co-fired) leadless chip carrier. CLCC is shown in the drawing on the next page.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and at different operating temperatures.

WARRANTY

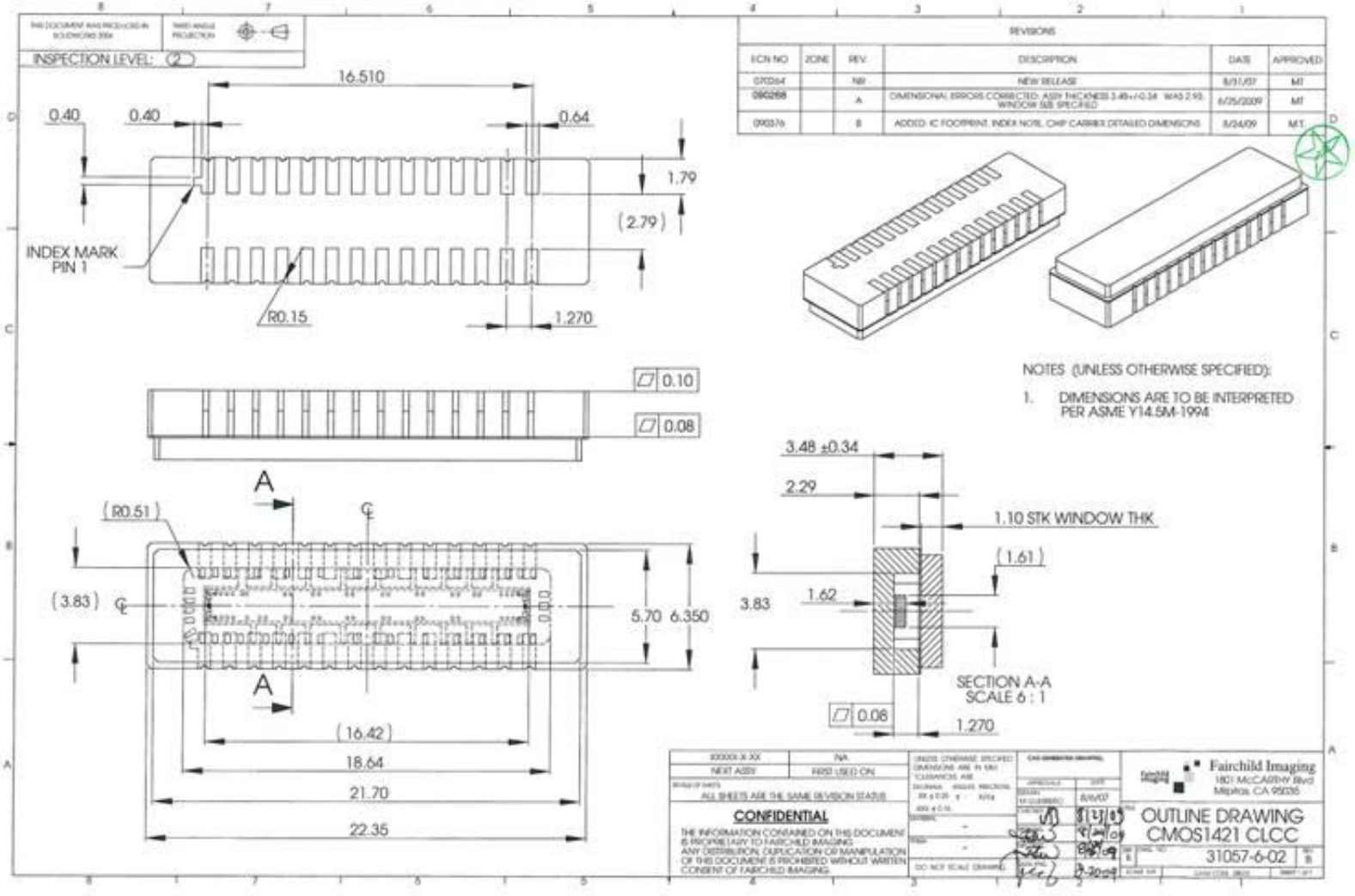
Fairchild Imaging warrants that its products will be free of defects in material and workmanship under normal use and service for one year from date of shipment

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System.

Fairchild Imaging
1801 McCarthy Blvd.,
Milpitas CA 95035
(800) 325-6975 or (408) 433-2500


INSPECTION LEVEL: 2
16.510
0.40
0.40
0.64
1.79
(2.79)
INDEX MARK
PIN 1
R0.15
1.270
0.10
0.08
A
(R0.51)
(3.83)
5.70
6.350
(16.42)
18.64
21.70
22.35
REVISIONS
NOTES (UNLESS OTHERWISE SPECIFIED):
1. DIMENSIONS ARE TO BE INTERPRETED PER ASME Y14.5M-1994
3.48 ±0.34
2.29
1.10 STK WINDOW THK
(1.61)
1.62
3.83
SECTION A-A
SCALE 6 : 1
0.06
1.270
CONFIDENTIAL
Fairchild Imaging
1801 McCARTHY Blvd
Milpitas, CA 95035
OUTLINE DRAWING
CMOS1421 CLCC
31057-6-02